## CLAIMS

What is claimed is:

1. A method of making a memory device, the method comprising:

forming a layer of material over the substrate, the layer of material is etch selective to a gate material;

forming an opening in the layer of material;

forming a first charge storage structure and a second charge storage structure, the first charge storage structure and the second charge storage structure formed by etching a layer of charge storage material through the opening to form an opening in the layer of charge storage material, wherein a first charge storage structure includes at least a portion of the layer of the charge storage material remaining after the etching and located on a first side of the opening in the layer of charge storage material and wherein a second charge storage structure includes at least a portion of the layer of the charge storage material remaining after the etching and located on a second side of the opening in the layer of charge storage material;

forming a gate, wherein the forming the gate includes depositing the gate material in the opening in the layer of material to form at least a portion of the gate,

wherein the portion of the gate includes a portion located over at least a portion of the first charge storage structure and over at least a portion of the second charge storage structure.

2. The method of claim 1 wherein a first side of the opening of the charge storage layer is aligned with a first side of the opening in the layer of material and the second side of the opening in the charge storing layer is aligned with a second side of the opening in the layer of material.

3. The method of claim 1 further comprising:
forming a first spacer in the opening in the layer of material;
forming a second spacer in the opening in the layer of material located apart from the first spacer by a space.

4. The method of claim 3 wherein the etching the layer of charge storage material further includes etching the layer of charge storage material through the space between the first spacer and the second spacer.

5. The method of claim 3 wherein the first spacer and the second spacer are formed from the layer of charge storing material.

6. The method of claim 3 further comprising:
wherein the first spacer is a side wall spacer formed on a first side of the opening in the layer of material and the second spacer is a side wall spacer formed on the second side of the opening in the layer of material.

7. The method of claim 3 further comprising:

implanting a dopant into the substrate through the space between the spacers to adjust a threshold voltage of the memory device.

8. The method of claim 3 wherein the first and second spacers include oxide.

9. The method of claim 3 wherein the first and second spacers include nitride.

10 10 The method of claim 3 wherein the first and second spacers include polysilicon.

11. The method of claim 10 wherein the gate includes at least a portion of the first spacer and at least a portion of the second spacer.

12. The method of claim 3 further comprising:

removing the first and second spacers after etching the layer of storage material.

13. The method of claim 3 wherein the etching the layer of the charge storage material through the opening includes etching the first spacer and the second spacer to reduce the first spacer and the second spacer to form the first charge storage structure and the second charge structure respectively, wherein the first charge storage structure is made from the first spacer and the second charge storage structure is made from the second spacer.

14. The method of claim 3 wherein:

the spacers are formed over the layer of charge storage material;

the first charge storage structure includes at least a portion of the layer of charge storing material located under the first spacer;

the second charge storage structure includes at least a portion of the layer of charge storing material located under the second spacer.

15. The method of claim 3 wherein the forming the first and second spacers further includes:

depositing a layer of spacer material comformally over the substrate;

anisotropically etching the layer of spacer material.

16. The method of claim 1 wherein the layer of charge storage material includes nitride.

17. The method of claim 1 wherein the layer of charge storage material includes

a plurality of discrete charge storage elements.

18. The method of claim 17 wherein each of the discrete charge storage elements includes clusters that include at least one of silicon, germanium, silicon carbide, and a metal.

19. The method of claim 1 wherein the layer of charge storage material includes at least one of hafnium oxide, tantalum oxide, aluminum oxide, zirconium oxide, hafnium silicate, lanthanum oxide, and hafnium aluminate.

20. The method of claim 1 further comprising:

forming a first layer of oxide over the semiconductor substrate;

forming a second layer of oxide over the semiconductor substrate and over the first layer of oxide, wherein a layer of charge storage material is located between the first layer of oxide and the second layer of oxide;

etching the second layer of oxide through the opening in the layer of material to form an opening in the second layer, wherein etching the layer of charge storage material includes etching the layer charge storage material through the opening in the second oxide layer.

21. The method of claim 20 further comprising:
etching the first layer of oxide through the opening in the second layer and through the opening in the layer of charge storing material to form on opening in the first layer.

22. The method of claim 21 further comprising:
forming oxide in the opening in the first layer.

23. The method of claim 1 wherein the layer of material is a dielectric material.

24. The method of claim 1 wherein the layer of charge storage material is formed before a formation of the layer of material.

25. The method of claim 1 wherein the layer of charge storage material is formed after the formation of the layer of material.

26. The method of claim 1 wherein the layer of material includes oxide.

27. The method of claim 1 wherein the layer of material includes nitride.

28. The method of claim 1 further comprising:
removing the layer of material after depositing the gate material.

29. The method of claim 28 wherein the forming the first charge storage structure and the second charge storage structure further includes:

etching the layer of charge storing material to remove portions of the layer of charge storing material located under the layer of material that is removed after depositing the gate material.

30. The method of claim 1 wherein the opening in the layer of material is formed by patterning the layer of material to form the opening.

31. A memory device comprising:

a substrate;

a gate located over the substrate;

a first charge storage structure located over an insulating layer on the substrate, at least a portion of the first charge structure located under a first portion of the gate,

a second charge storage structure located over the substrate, at least a portion of the second charge storage structure located under a second portion of the gate, the second charge storage structure is located apart from the first charge storage structure.

wherein the gate includes a third portion located between the first portion of the gate and the second portion of the gate;

a gate dielectric, a first portion of the gate dielectric located between the substrate and the first charge storage structure, a second portion of the gate dielectric located between the substrate and the second

charge storage structure, a third portion of the gate dielectric located between the substrate and the third portion of the gate, wherein the third portion of the gate dielectric at a location where the gate is closest to the substrate, has a thickness that is different from a thickness of first portion of the gate dielectric and a thickness of the second portion of the gate dielectric.

32. The memory device of claim 31 wherein the thickness of the third portion of the gate dielectric at the location is less than the thickness of the first portion of the gate dielectric and less than the thickness of the second portion of the gate dielectric.

33. The memory device of claim 31 wherein the thickness of the third portion of the gate dielectric at the location is greater than the thickness of the first portion of the gate dielectric and is greater than the thickness of the second portion of the gate dielectric.

34. The memory device of claim 31 wherein the first charge storage structure and the second charge storage structure each include a plurality of discrete charge storage elements.

35. The memory device of claim 31 wherein a width of the first charge storing structure and a width of the second charge storing structure is less than a minimum feature size.

36. The device of claim 31 wherein each of the first and second charge storage structures is for storing one bit of information.

37. A method of making a memory device, the method comprising:

forming a layer of material over the substrate and over a layer of charge storage material;

patterning an opening in the layer of material;

forming a first side-wall spacer on a first side of the opening over the layer of charge storage material;

forming a second side-wall spacer on a second side of the opening over the layer of charge storage material, the first side wall spacer spaced apart from the second side-wall spacer by a space;

forming a first charge storage structure and a second charge storage structure, the forming the first charge storage structure and the second charge storage structure includes etching the layer of the charge storage material through the space between the first side-wall spacer and the second side-wall spacer to form an opening in the layer of charge storage material, wherein a first charge storage structure includes at least a portion of the layer of the charge storage material located under the first side-wall spacer and remaining after the etching and a second charge storage structure includes at least a portion of the layer of the charge storage material located under the second side-wall spacer and remaining after the etching;

forming a gate, wherein the gate includes a portion located over at least a portion of the first charge storage structure and a portion located over at least a portion of the second charge storage structure.

38. The method of claim 37 wherein the gate includes at least a portion of the first spacer and at least a portion of the second spacer.

39. The method of claim 37 further wherein the forming the gate further includes depositing a gate material in the opening in the layer of material, the method further comprising:

removing the layer of material after depositing the gate material;

wherein the forming the first charge storage structure and the second charge storage structure further includes etching the layer of charge storing material to remove portions of the layer of charge storing material located under the layer of material removed that is removed after depositing the gate material.